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JAN 94 U.S. PTO

**NEW UTILITY PATENT APPLICATION TRANSMITTAL  
(Large Entity)***(Only for new nonprovisional applications under 37 CFR 1.53(b))*Docket No.  
29131.0217Total Pages in this Submission  
3**TO THE ASSISTANT COMMISSIONER FOR PATENTS**Box Patent Application  
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

**METHODS AND APPARATUS FOR THE CHEMICAL MECHANICAL PLANARIZATION OF ELECTRONIC DEVICES**

and invented by:

**CLINTON O. FRUITMAN**If a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:☒ Continuation    ☐ Divisional    ☐ Continuation-in-part (CIP)    of prior application No.: 08/662,678

Enclosed are:

**Application Elements**

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 8 pages and including the following:
  - a. ☒ Descriptive Title of the Invention
  - b. ☐ Cross References to Related Applications *(if applicable)*
  - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
  - d. ☐ Reference to Microfiche Appendix *(if applicable)*
  - e. ☒ Background of the Invention
  - f. ☒ Brief Summary of the Invention
  - g. ☒ Brief Description of the Drawings *(if drawings filed)*
  - h. ☒ Detailed Description
  - i. ☒ Claim(s) as Classified Below
  - j. ☐ Abstract of the Disclosure
3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
  - a. ☐ Formal
  - b. ☒ Informal

Number of Sheets 5

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3

**Application Elements (Continued)**

4. ☒ Oath or Declaration
- a. ☐ Newly executed (*original or copy*)      ☐ Unexecuted
- b. ☒ Copy from a prior application (37 CFR 1.63(d)) (*for continuation/divisional application only*)
- c. ☒ With Power of Attorney      ☐ Without Power of Attorney
5. ☒ Incorporation By Reference (*usable if Box 4b is checked*)  
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche (*Appendix*)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all must be included*)
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy (*identical to computer copy*)
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

**Accompanying Application Parts**

8. ☐ Assignment Papers (*cover sheet & document(s)*)
9. ☐ 37 CFR 3.73(B) Statement (*when there is an assignee*)
10. ☐ English Translation Document (*if applicable*)
11. ☒ Information Disclosure Statement/PTO-1449      ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
- ☐ First Class      ☒ Express Mail (*Specify Label No.*): EM 339 509 795 US
15. ☐ Certified Copy of Priority Document(s) (*if foreign priority is claimed*)

# NEW UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.  
29131.0217

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3

## Accompanying Application Parts (Continued)

16. ☐ Additional Enclosures (please identify below):

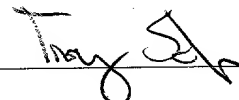
## Fee Calculation and Transmittal

### CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	3	- 20 =	0	x \$22.00	\$0.00
Indep. Claims	3	- 3 =	0	x \$82.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$790.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$790.00

- ☒ A check in the amount of \$790.00 to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Dated: JANUARY 16, 1998

 Signature

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REG. NO. 36,667

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cc:

**CERTIFICATE OF MAILING BY U.S. EXPRESS MAIL NO. EM 339 509 795 US**

I hereby certify that the attached Continuation Patent Application, with attachments (if any), pursuant to 37 C.F.R. §111 and 37 C.F.R. §1.53 is being deposited as U.S. Express Mail this date with the United States Postal Service in an envelope addressed to the Assistant Commissioner of Patents, Box New Application, Washington, D.C. 20231, on

Date: January 16, 1998

By: \_\_\_\_\_

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Margarete E. Adams

Atty Docket No.: 29131.0217

# METHODS AND APPARATUS FOR THE CHEMICAL MECHANICAL PLANARIZATION OF ELECTRONIC DEVICES

5 Inventor: Clinton O. Fruitman

## Technical Field

10 The present invention relates, generally, to methods and apparatus for the planarization and fine finishing of flat surfaces in the microelectronics industry and, more particularly, to the use of a substantially flat, non-cellular pad in a chemical mechanical planarization (CMP) process.

## Background Art and Technical Problems

15 Chemical mechanical planarization ("CMP") is widely used in the microelectronics industry. A typical CMP process involves polishing back built up insulating layers of insulators or conductors on integrated circuit chips during manufacture.

20 More particularly, a resinous polishing pad having a cellular structure is employed in conjunction with a slurry, for example a water-based slurry comprising colloidal silica particles. When pressure is applied between the polishing pad in the workpiece (e.g., silicon wafer) being polished, mechanical stresses are concentrated on the exposed edges of the adjoining cells in the cellular pad. Abrasive particles within the slurry concentrated on these edges tend to create zones of localized high stress at the workpiece in the vicinity of the  
25 exposed edges of the polishing pad. This localized pressure creates mechanical strain on the chemical bonds comprising the surface being polished, rendering the chemical bonds more susceptible to chemical attack or corrosion (e.g., stress corrosion). Consequently, microscopic regions are removed from the surface being polished, enhancing planarity of the polished surface. See, for example, *Arai, et al.*, U.S. Patent No. 5,099,614, issued March, 1992; *Karlsru*  
30 *et al.*, U.S. Patent No. 5,498,196, issued March, 1996; *Arai, et al.*, U.S. Patent No. 4,805,348, issued February, 1989; *Karlsru et al.*, U.S. Patent No. 5,329,732, issued July, 1994; and *Karlsru et al.*, U.S. Patent No. 5,498,199, issued March, 1996. For a further discussion of presently known lapping and planarization techniques. By this reference, the entire disclosures of the foregoing patents are hereby incorporated herein.

Presently known polishing techniques are unsatisfactory in several regards. For example, as the size of microelectronic structures used in integrated circuits decreases, and further as the number of microelectronic structures on current and future generation integrated circuits increases, the degree of planarity required increases dramatically. For example, the high degree of accuracy of current lithographic techniques or smaller devices requires increasingly flatter surfaces. Presently known polishing techniques are believed to be inadequate to produce the degree of planarity and uniformity across the relatively large surfaces of silicon wafers used in integrated circuits, particularly for future generations.

Presently known polishing techniques are also unsatisfactory in that the cellular structure of the polishing pad tends to generate heat at the interface between the pad and the workpiece. The presence of heat is problematic in that it tends to dry the slurry in the vicinity of large workpiece centers. As a polishing pad moves radially inward across the surface of a circular wafer, it has been observed that the slurry can dehydrate unevenly across the surface of the workpiece. Consequently, the polishing effect of the pad can be non-uniform across the surface of the workpiece, resulting in non-uniform planarization effects.

Chemical mechanical planarization techniques and materials are thus needed which will permit a higher degree of planarization and uniformity of that planarization over the entire surface of integrated circuit structures.

### Summary of the Invention

In accordance with a preferred exemplary embodiment of the present invention, a chemical mechanical planarization process employs a non-cellular surface or pad in lieu of the traditional cellular polishing pad employed in presently known CMP processes. Such a flat or non-cellular pad dramatically reduces the number of stress concentration points over a given surface area of contact between the polishing pad and the workpiece being polished, resulting in a more uniform planarization across the workpiece surface. In accordance with a further aspect of the present invention, the use of a non-cellular pad also may have the effect of reducing the extent to which the pad bends over device topographies due to the lack of a cellular nap. In accordance with a further aspect of the present invention, to the extent the reduction in asperity density (number of stress concentration points per surface area at the polishing pad) reduces the material removal rate in the polishing process, the pressure between the polishing pad and workpiece may be increased to thereby compensate for the reduction

removal rate. Inasmuch as the increased pressure will be spread out over a greater surface area of contact between the pad and the workpiece, damage to delicate microstructures may be concomitantly minimized.

In accordance with a further aspect of the present invention, the use of a non-cellular or substantially flat polishing pad effectively performs a lapping function on the workpiece, to the extent contact forces are distributed over a greater area for a given applied pressure, achieving maximum flatness and planarity on the workpieces being polished.

In accordance with a further aspect of the present invention, use of a non-cellular and/or substantially flat pad in lieu of the traditional cellular polishing pads facilitates more uniform slurry distribution, reducing non-uniform effects of planarization on the finished workpieces.

### Brief Description of the Drawing Figures

The subject invention will hereinafter be described in conjunction with the appended drawing figures, wherein like numerals designate like elements, and:

Figure 1 is a schematic diagram of an exemplary foam polishing pad operating on an exemplary silicon workpiece in an abrasive slurry environment;

Figure 2 is a concept diagram illustrating chemical aspects of a traditional chemical mechanical planarization process;

Figure 3 is a close-up view of an exemplary known polishing pad, showing stress concentration points;

Figure 4(a) is a schematic cross-section view of an exemplary section of an integrated circuit, showing microelectronic structures imbedded in a dielectric layer, shown in conjunction with a presently known polishing pad;

Figure 4(b) is a schematic representation of the structure of Figure 4(a) upon completion of a presently known polishing process, illustrating localized non-planarity;

Figure 5(a) is a schematic cross-section view of a non-cellular pad in accordance with a preferred embodiment of the present invention; and

Figure 5(b) is a schematic cross-section view of the structure of Figure 5(a) illustrating the enhanced planarity achievable with the substantially flat "lapping" pad of the present invention.

### Detailed Description of Preferred Exemplary Embodiments

Referring now to Figure 1, presently known CMP processes typically employ a rigid foam polishing pad 10 to polish the surface of a workpiece 12, for example an integrated circuit layer. An abrasive slurry comprising a plurality of abrasive particles 14 in an aqueous medium is employed at the interface between the pad surface and workpiece surface.

With momentary reference to **Figures 1 and 3**, cellular pad 10 comprises a large number of randomly distributed open cells or bubbles, with exposed, irregularly shaped edges forming the junction between cells. Those edge surfaces 16 which come into contact with surface 18 of workpiece 12 are known as asperities, and support the load applied to pad 10 which results in frictional forces between pad 10 and workpiece 12 as pad 10 is moved laterally (e.g., in a circular planatary manner) with respect to workpiece 12 during the polishing process.

With continued reference to **Figures 1 and 3**, abrasive particles 14 within the slurry are urged onto surface 18 of workpiece 12 by asperities 16, creating high stress concentrations at the contact regions between asperities 16 and surface 18. Thus, **Figure 1** illustrates some of the principle mechanical phenomena associated with known CMP processes.

Referring now to **Figure 2**, some of the principle chemical phenomena associated with known CMP techniques are illustrated. For example, in the case of polishing silica dielectrics, an ownwardly and impressed onto surface 18 of workpiece 12 by the pad, the chemical bonds which make up the structure of that layer of workpiece 12 in contact with pad 10 become mechanically stressed. The mechanical stress applied to these chemical bonds and their resultant strain increases the affinity of these bonds for hydroxide groups which are attached to abrasive particle 14. When the chemical bonds which comprise surface 18 of workpiece 12 are broken, silanols are liberated from surface 18 and carried away by the slurry. The liberation of these surface compounds facilitates the creation of a smooth, flat, highly planar surface 18.

In the context of a preferred embodiment of the present invention, a slurry is used to effect the chemical/mechanical polishing and planarization effects. More particularly, in the context of the present invention, a "slurry" suitably comprises a chemically and mechanically active solution, for example including abrasive particles coupled with chemically reactive agents. Suitable chemically reactive agents include hydroxides, but may also include highly basic or highly acidic ions: Suitable agents (e.g., hydroxides) are advantageously coupled to the abrasive particles within the slurry solution. In the context of a particularly preferred

embodiment, suitable abrasive particles within the slurry may be on the order of 10-200 nanometers in size in the source (dry) state, and most preferably about 30-80 nanometers. This is in contrast to traditional lapping solutions, which may include abrasives having sizes in the range of 0.5-100 micrometers. Suitable slurries in the context of the present invention may also include oxidizing agents (e.g., potassium fluoride), for example in a concentration on the order of 5-20% by weight particle density, and most preferably about 11% by weight particle density.

Referring now to Figures 3 and 4(a), an exemplary workpiece 12 suitably comprises a silicon layer 22 having microelectronic structures 24 disposed thereon (or therein). In accordance with the illustrated embodiment, microstructures 24 may comprise conductors, via holes, or the like, in the context of an integrated circuit. Workpiece 12 further comprises a dielectric layer 20 applied to the surface of silicon layer 22, which dielectric layer may function as an insulator between successive silicon layers in a multiple-layered integrated circuit.

During the semi-conductor manufacture process, dielectric 20 is placed over silicon layer 22 (and its associated electronic microstructures) in such a way that localized device topographies (e.g., ridges) 26 are formed in the dielectric layer corresponding to microstructures 24. It is these ridges, inter alia, which need to be eliminated during the CMP process to form an ideally uniform, flat, planar surface upon completion the CMP process. However, as is known in the art, present CMP techniques are not always capable of producing a sufficiently flat, planar surface, particularly for small device lithography, for example in the submicrometer (e.g., less than 2.5 micrometer) range.

Referring now to Figures 4(a) and 4(b), the asperities (e.g., projections) associated with the undersurface of polishing pad 10 contact dielectric surface 20 as surface 20 and pad 10 are moved relative to one another during the polishing process. A chemically and mechanically active slurry or other suitable solution (not shown in Figure 4) is provided between the mating surfaces of workpiece 12 and pad 10 to facilitate the polishing process. As pad 10 moves relative to workpiece 12, the asperities associated with pad 10, in conjunction with the abrasive particles comprising the slurry, polish down device topographies (ridges) 26, removing material from the ridges in accordance with the chemical and mechanical phenomena associated with the CMP process described above. In particular, the irregular edges which form the surfaces adjoining the cells of pad 10 tend to deflect or bend as they encounter

respective leading edges 28 of ridges 26, trapping abrasive particles between the asperities associated with pad 10 and the edges of respective device topographies 26, wearing down respective edges 28 at a faster rate than the device topography surfaces. During the course of the polishing process, ridges 26 are typically worn down until they are substantially co-planar with surface 18; however, it is known that this planarization process is incomplete. Hence, residual nodes or undulations 30 typically remain proximate microstructures 24 upon completion of the planarization process. Although surface 18(b) associated with workpiece 12 is certainly more highly planar upon completion of the CMP process than the surface 18(a) associated with workpiece 12 prior to completion of the planarization process, the existence of nodules can nonetheless be problematic, particularly in future generation integrated circuits wherein extremely high degrees of planarity are desired.

Referring now to **Figure 5**, a "lapping" pad 31 is suitably employed in a CMP process in lieu of polishing pad 10. In accordance with a particularly preferred embodiment, pad 31 suitably comprises a substantially flat surface in contact with workpiece 12, characterized by relatively few surface irregularities 34. In particular, surface irregularities 34 may comprise scratches or other non-planarities associated with the dressing of pad 31; alternatively, irregularities 34 may simply result from the welding together of polymers comprising pad 31, *e.g.*, fused polyethylene, non-cellular urethanes, and the like.

In accordance with a further aspect of the present invention, pad 30 is suitably made from a porous material, which permits the adsorption and/or entrainment of suitable slurries, for example, aqueous high pH slurries comprising colloidal silica such as SC1 manufactured by the Cabot Corp. or Deltapol 4101 manufactured by SpeedFam Corporation of Chandler, Arizona, or cerium oxide slurried or low pH alumina slurries. In accordance with yet a further aspect of the present invention, pad 30 may suitably comprise any suitable flat material soft enough to resist damage to fragile integrated circuit device layers, *e.g.*, flexibilized, epoxies. In this regard, it is desirable that pad 30 be desirably relatively pliable to permit the undersurface of pad 31 to conform to the global topography of a workpiece (*e.g.*, wafers) without damaging the delicate microstructures 24 associated with workpiece 12 as pressures are applied between pad 31 and workpiece 12.

With continued reference to **Figure 5**, as pad 31 is moved laterally relative to workpiece 12, the downward force of pad 31 and, hence, the lateral shearing forces created at the interface between workpiece 12 and pad 31 are spread out over a substantially larger

surface area than was the case with pad 10. Consequently, substantially higher pressures may be applied between workpiece 12 and pad 31 than could be applied between workpiece 12 and pad 10 (see, Figure 4) without damaging the surface of workpiece 12 (e.g., microstructures 24). Moreover, the flat surface 32 of pad 31; as opposed to the asperities 16 associated with pad 10, urge particles 14 onto surface 18 more uniformly, thereby resulting in a more uniform planar surface 18(b), as shown in Figure 5(b). Indeed, the use of a non-cellular or otherwise substantially flat surface associated with pad 31 greatly reduces the step height of the device microstructures associated with planarized surfaces 18(b).

Although the present invention is set forth herein in the context of the appended drawing figures, it should be appreciated that the invention to the specific forms shown. Various other modifications, variations, and enhancements in the design an arrangement of the non-cellular pad and various process parameters discussed herein may be made without departing from the spirit and scope of the present invention as set forth in the appended claims. For example, a preferred embodiment of the present invention is illustrated herein in the context of a dielectric layer over microelectronic structures; however, the present invention may be useful in the context of both multilevel integrated circuits and other small electronic devices, and for fine finishing, flattening and planarization of a broad variety of chemical, electro-mechanical, electromagnetic, resistive and inductive resistive devices, as well as for the fine finishing, flattening and planarization of optical and electro-optical and mechanical devices. These and other modifications may be made in the design and implementation of various aspects of the invention without departing from the spirit and scope of the invention as set forth in the appended claims.

*CLAIMS:*

1. An improved chemical mechanical planarization process involving the use of a polishing pad in conjunction with an abrasive slurry to wear down surface topographies in a dielectric layer of an integrated circuit workpiece, the improvement comprising:

the step of employing a non-cellular lapping pad in lieu of a cellular polishing pad.

2. A system for polishing the surface of a workpiece, comprising:

a fixture for mounting said workpiece to thereby expose a first surface of said workpiece;

a second fixture for mounting a polishing pad movable into contact with said first surface of said workpiece under pressure in the presence of an abrasive slurry; and

a substantially flat, non-cellular polishing pad disposed in said second fixture.

3. A process for polishing substantially flat workpiece surfaces, comprising the steps of:

providing a substantially, non-cellular polishing pad;

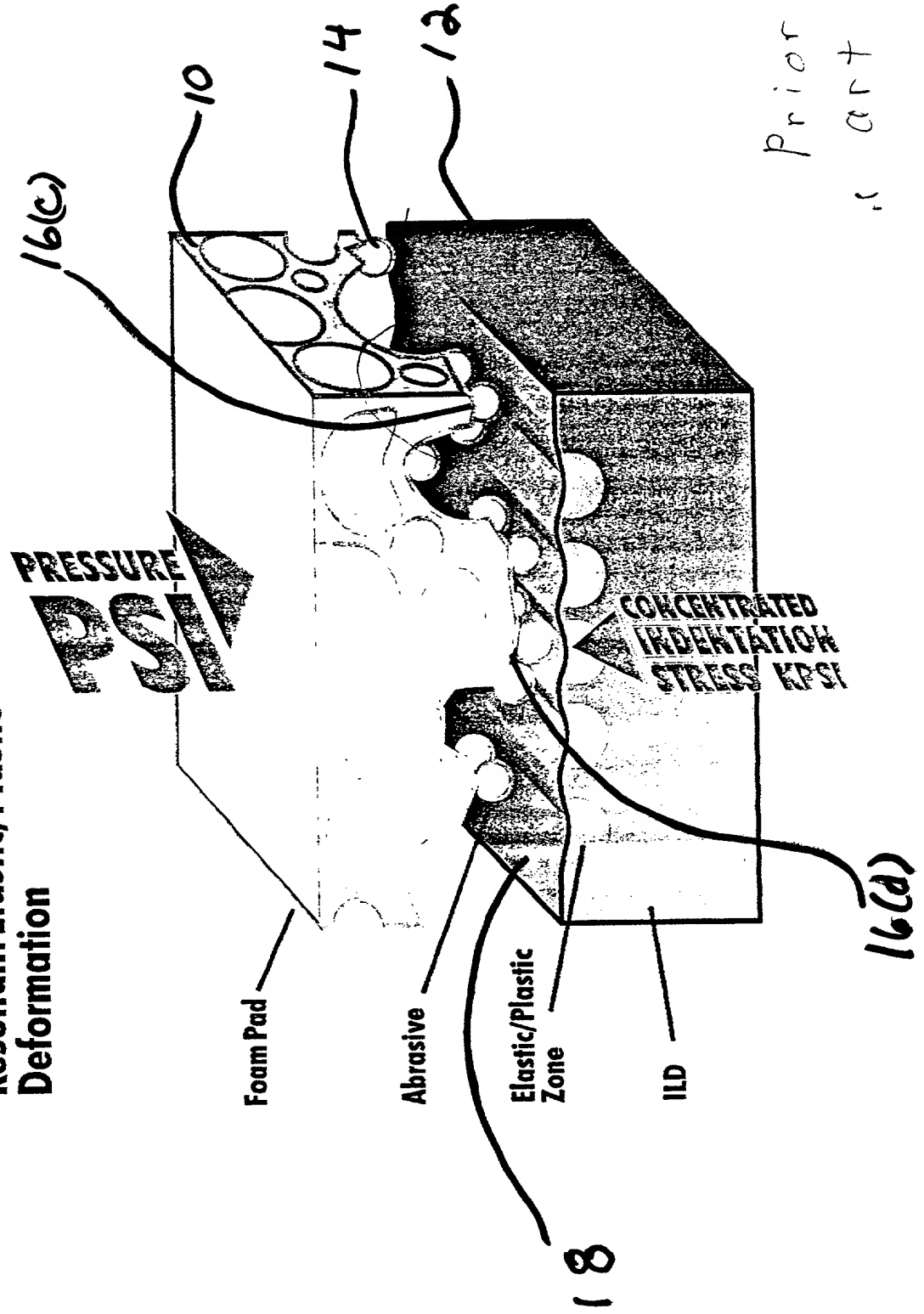
applying said pad under pressure to said workpiece surface in the presence of a chemical mechanical polishing slurry; and

relatively moving said pad with respect to said workpiece surface along a plurality of directions within the plane defined by the mating surface between said pad and said workpiece.

FIG 1

# MECHANICAL COMPONENT

Stress Concentration and  
Resultant Elastic/Plastic  
Deformation



# CHEMICAL COMPONENT

## Double Layer of OH<sup>-</sup> on Abrasive is the Contact Source for Silanol Bond Formation

FIG. 2

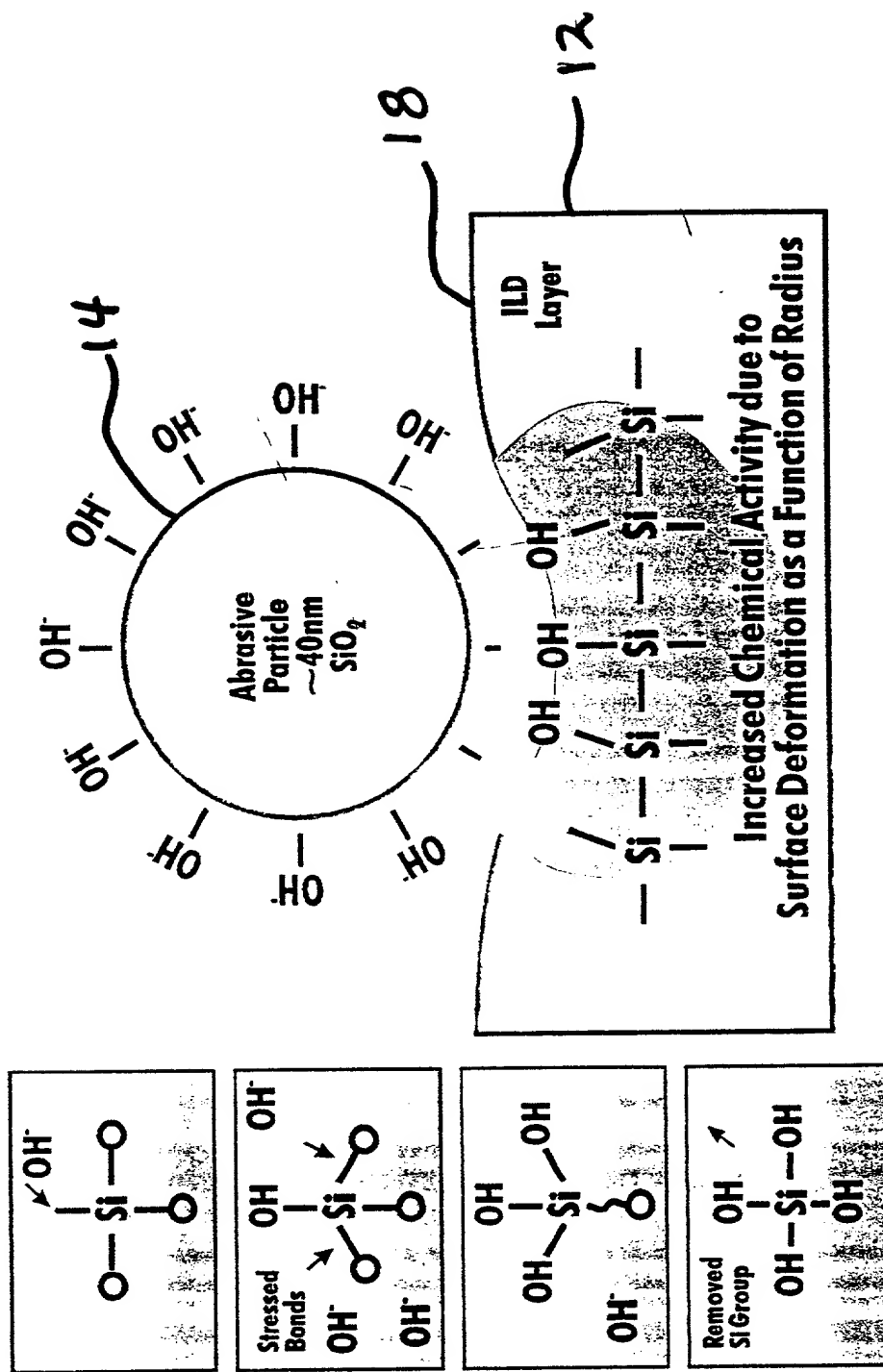
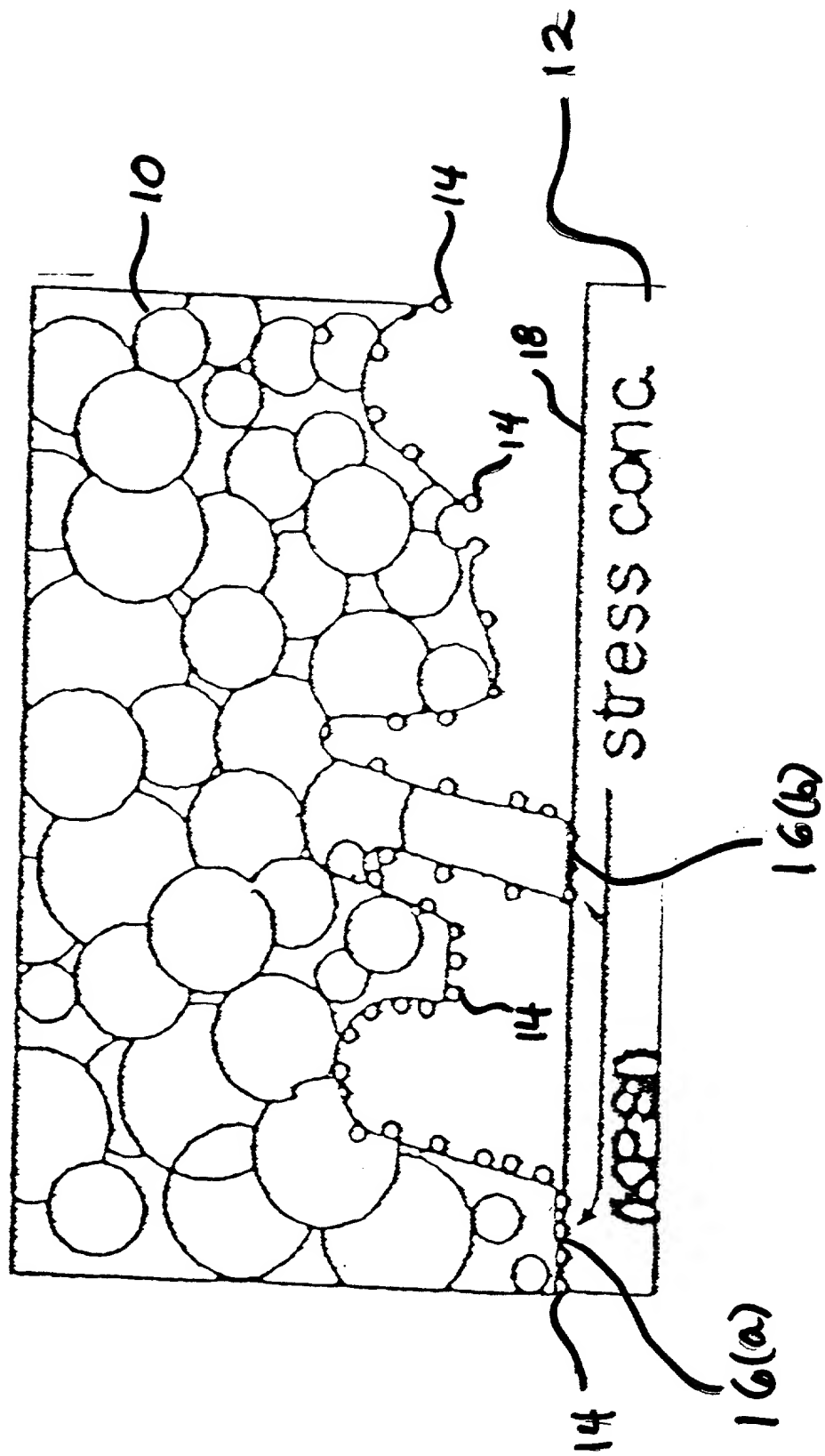


FIG 3



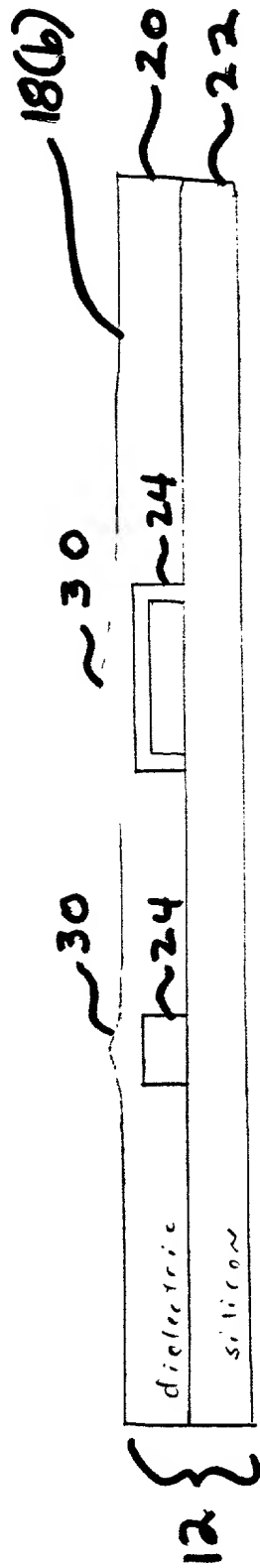
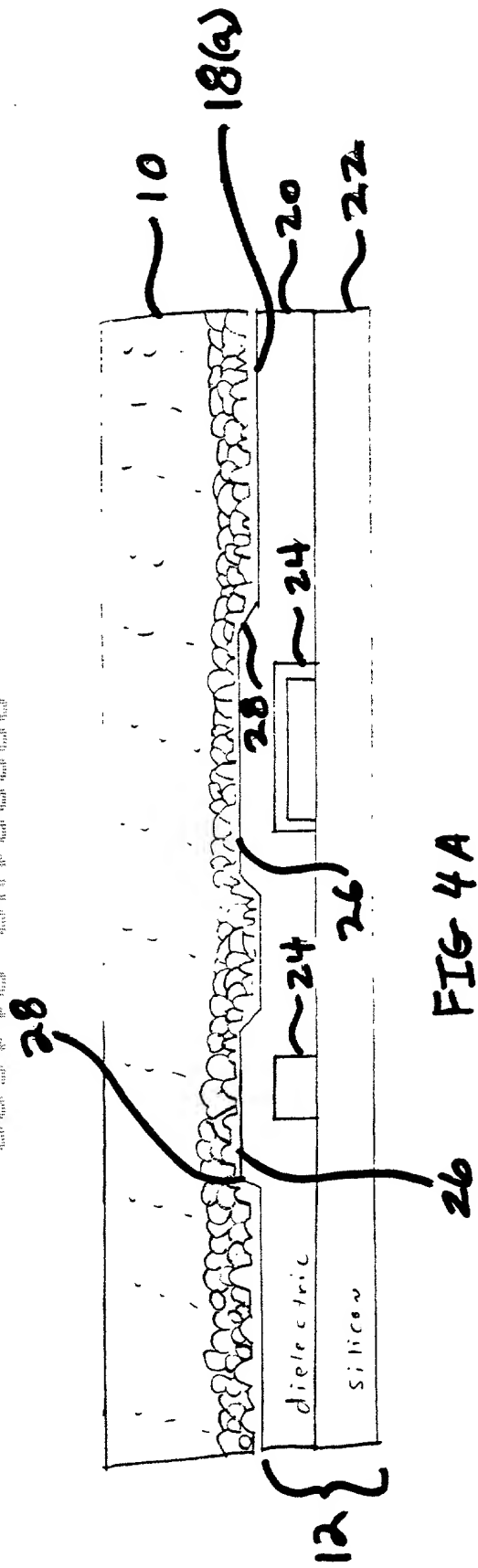


FIG 4B

	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431	2432	2433	2434	2435	2436	2437	2438	2439	2440</
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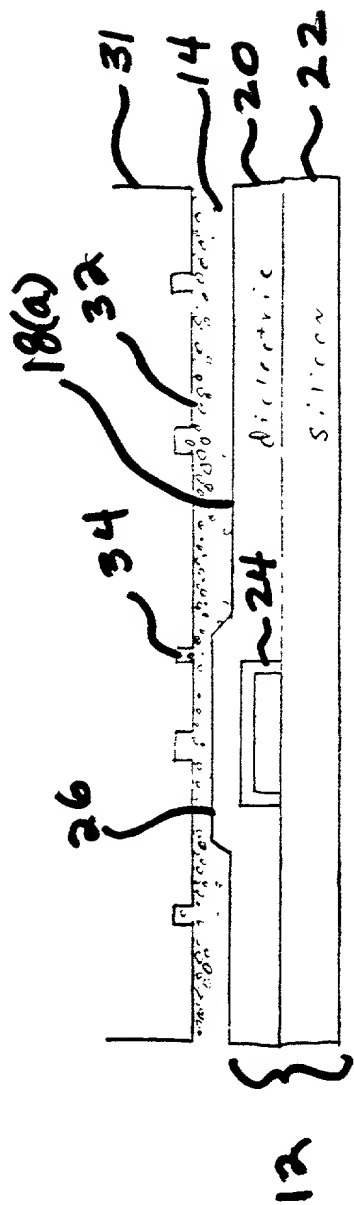
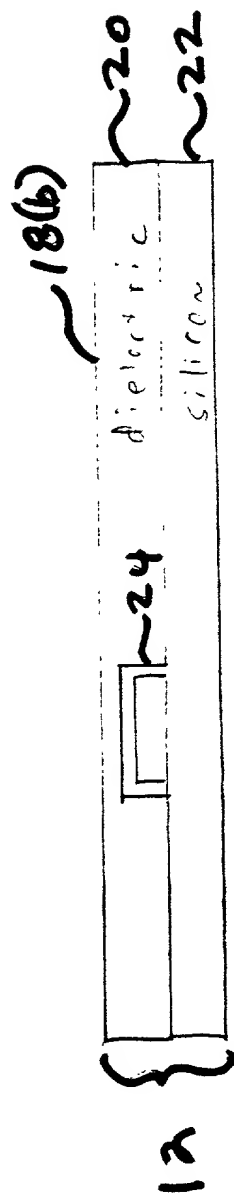


FIG 5A



## DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare: THAT my residence, post office address and citizenship are as stated below next to my name; THAT I verily believe I am the inventor of the invention entitled: **METHODS AND APPARATUS FOR THE CHEMICAL MECHANICAL PLANARIZATION OF ELECTRONIC DEVICES**, for which application for Letters Patent of the United States was filed as a new patent application on June 14, 1996.

THAT I do not know and do not believe that this invention was ever known or used in the United States of America before my invention or discovery thereof, or patented or described in any printed publication in any country before my invention or discovery thereof, more than one year prior to this application;

THAT the invention was not in public use or on sale in the United States of America for more than one year prior to this application;

THAT this invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months before this application;

THAT I have reviewed and understand the contents of the above identified specification, including the claim(s), as amended by any amendment referred to above;

THAT I acknowledge the duty to disclose information of which I am aware which is material to the examination of this application in accordance with 37 C.F.R. §1.56; and

THAT no applications for patent or inventor's certificate on this invention or discovery have been filed by me or my legal representatives or assigns in any country foreign to the United States of America.

And I hereby appoint, as my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, individually and collectively:

**SNELL & WILMER LLP.**  
One Arizona Center  
400 East Van Buren  
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Fax (602) 382-6070

**ATTENTION:**  
**MICHAEL K. KELLY**

(to whom all communications regarding the subject application are to be directed); and each attorney thereof named below with Registration Numbers, and of the same address:

Sherman O. Parrett	Reg. No. 25,905	Michael K. Kelly	Reg. No. 32,848
Charles F. Hauff, Jr.	Reg. No. 33,244	Howard Sobelman	Reg. No. 39,038
Daniel J. Noblitt	Reg. No. 35,969	Sharon K. Coleman	Reg. No. 39,148
Kevin LeMond	Reg. No. 35,933		

Please send all further correspondence to Snell & Wilmer L.L.P. at the foregoing address.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

(1) Inventor's Signature Clinton O. Fruitman  
Date 6/14/96 Inventor's Name (typed) Clinton O. Fruitman  
Citizenship United States of America  
Residence (City) Chandler (State/Foreign Country) AZ  
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